Test cases

\*Assuming a clock period of 10

|  |  |  |
| --- | --- | --- |
| Design | Timing Report Without SPEF | Timing Report With SPEF |
| Crc32 | 7.16 | 0.21 |
| Spi\_master | 3.57 | 3.45 |
| Rle\_enc | 7.47 | 5.45 |
| Uart | 6.87 | 4.23 |
| Cpu | 2.84 | -15.17 |

All the SPEF files are syntax-error free